AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A margin testing system for margin testing one or more components of an electronic system, comprising:

a fault bypass module incorporated in said electronic system, said fault bypass module configured to intercept and mask signals indicative of one or more faults associated with one or more of said components during margin testing of said electronic system.

2. (Previously Presented) The margin testing system of claim 1, wherein at least one of said one or more faults corresponds to an operating parameter associated with at least one of said one or more components crossing a selected threshold.

3. (Original) The margin testing system of claim 2, wherein said operating parameter is any of frequency, voltage or temperature.

4. (Previously Presented) The margin testing system of claim 1, further comprising:

a controller incorporated in said electronic system and in communication with said fault bypass module, said controller configured to transmit a command to said fault bypass module to initiate masking of said fault signals by said module.

5. (Previously Presented) The margin testing system of claim 1, wherein said fault signals comprise:

one or more interrupt signals.

6. (Original) The margin testing system of claim 1, wherein said fault bypass module permits normal processing of said fault signals during normal operation of said electronic system.

7. (Previously Presented) The margin testing system of claim 4, further comprising:

a hardware monitor configured to communicate with said controller and with at least one of said one or more components, and to generate a fault signal in response to an occurrence of a fault associated with said at least one component.

8. (Previously Presented) The margin testing system of claim 7, wherein said hardware monitor is further configured to transmit said fault signal to said fault bypass module, and wherein said fault bypass module is further configured to mask said received fault signal during margin testing of said electronic device.

9. (Previously Presented) The margin testing system of claim 1, further comprising:

a power control element configured to communicate with said fault bypass module, and wherein said fault bypass module is further configured to transmit one or of more of said fault signals to said power control element in absence of margin testing and to mask said one or more fault signals during margin testing of said electronic system.

10. (Previously Presented) The margin testing system of claim 9, wherein said fault bypass module is further configured to mask said fault signal by intercepting said fault signal and supplying to said power control element a signal indicative of an absence of a fault indicated by said fault signal.

11. (Previously Presented) The margin testing system of claim 7, wherein said at least one component is a power rail, and said hardware monitor is further configured to generate an interrupt signal in response to a voltage associated with said power rail varying from a nominal value by more than a selected threshold.

12. (Previously Presented) The margin testing system of claim 11, wherein said power control module is further configured to reduce power applied to said power rail in response to said interrupt signal in the absence of margin testing.

13. (Original) The margin testing system of claim 1, wherein said fault bypass module comprises:

a programmable logic device programmed to provide masking of said fault signals.

14. (Previously Presented) The margin testing system of claim 7, further comprising

a temperature diode coupled to at least one of said components and configured to measure a temperature of said component and to supply said measured temperature to said hardware monitor.

15. (Previously Presented) The margin testing system of claim 7, wherein said fault bypass module is further configured to intercept a selected output signal of said at least one component and to generate a simulated signal corresponding to said intercepted output signal for transmittal to said hardware monitor during margin testing of said component.

16. (Original) The margin testing system of claim 1, wherein said electronic system comprises a computer system.

17. (Original) The margin testing system of claim 15, wherein said computer system is a computer server.

18. (Previously Presented) The margin testing system of claim 4, wherein said controller comprises:

a Baseboard Management Controller (BMC).

19. (Original) The margin testing system of claim 18, further comprising:

a communication bus for providing communication between said BMC and said fault bypass module.

20. (Previously Presented) The margin testing system of claim 19, wherein said communication bus is an Inter-Integrated Circuit (I^2C)-based bus.

21. (Previously Presented) The margin testing system of claim 20, wherein said I^2C bus is an Intelligent Platform Management Bus (IPMB).

22. (Previously Presented) A electronic system comprising a margin testing system for margin testing one or more components of the electronic system, said margin testing system comprising:

a fault bypass module incorporated in said electronic system, said fault bypass module configured to intercept and mask signals indicative of one or more faults associated with one or more of said components during margin testing of said electronic system; and

an internal controller in communication with said fault bypass module, said internal controller configured to transmit a command to said fault bypass module to initiate masking of said fault signals by said module.

23. (Previously Presented) The electronic system of claim 22, wherein said controller is a Baseboard Management Controller (BMC).

24. (Previously Presented) A method of masking faults during margin testing of an electronic system, comprising:

intercepting one or more signals each indicative of one or more faults associated with one or more components of said electronic system during margin testing thereof; and

generating signals indicative of absence of said faults, thereby masking said intercepted signals.

25. (Previously Presented) The method of claim 24, further comprising:

transmitting at least one of said one or more fault signals to a power control element in absence of margin testing.

26. (Previously Presented) The method of claim 25, wherein masking said intercepted signals, comprises:

supplying to said power control element a signal indicative of absence of a fault indicated by said fault signals.

27. (Previously Presented) The method of claim 24, further comprising:

generating an interrupt signal in response to a voltage associated with a power rail varying from a nominal value by more than a selected threshold.

28. (Currently Amended) The method ~~margin testing system~~ of claim 27, further comprising:

reducing power applied to said power rail in response to said interrupt signal in the absence of margin testing.

29. (Previously Presented) The method claim 24, wherein intercepting one or more signals, comprises:

intercepting a selected output signal of said one or more components; and

wherein generating signals indicative of absence of said faults, comprises:

generating a simulated signal corresponding to said intercepted output signal for transmittal to a hardware monitor.

30. (Previously Presented) The method of claim 24, wherein said electronic system is a computer server.

31. (Previously Presented) A system comprising:

means for intercepting at least one signal indicative of at least one fault associated with at least one component of an electronic system during margin testing thereof; and

means for masking said intercepted at least one signal by generating at least one signal indicative of absence of said at least one fault.

32. (Previously Presented) A computer server, comprising a margin testing system for margin testing one or more components of the computer server, the margin testing system comprising:

a fault bypass module incorporated in said computer server, said fault bypass module configured to mask signals indicative of one or more faults associated with one or more of said components during margin testing of said computer server.